

## **REMARKS**

The Examiner is thanked for the thorough examination of the present application and the withdrawal of previous rejections. The Office Action, however, continued to reject all claims 1-16. In response thereto, Applicants submit the foregoing amendments and the following remarks.

In this regard, claims 1, 6, 9, and 14 have been amended in order to expedite the examination of the present application. In this regard, independent claims 1 and 9 have been amended to incorporate the subject matter of claims 5 and 13, respectively. Claims 5 and 13 are accordingly canceled. Applicants make these amendments without prejudice, waiver, disclaimer, or dedication of any subject matter embodied in the previous version of the claims. The amended claims are supported by the previous version of the claims, as well as Fig. 3 and paragraphs [0020] to [0024] of the detailed description. Accordingly, no new matter has been added to the application by these amendments.

Claims 1-4, 6-12, and 14-16 are currently pending in the present application. Applicant respectfully requests reconsideration of these claims.

### **Claim Objection – Clarification**

With regard to the claim objection to claim 9, Applicant hereby confirms that the word “not” was intended to be inserted with the last response, in accordance with the Examiner’s suggestion. The use of the double-brackets around that were was inadvertent.

## **Claim Rejections**

The Office Action rejected claims 1, 2, 4, 5, 7-10, 12, 13, 15, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over the combination of Isley in view of Robinson, Joshi, and Dent.

The rejections are based on the selective combination of four different references to establish that the presently claimed joint clock source coupling architecture has been disclosed. Applicant respectfully traverses this rejection, as it is Applicant's belief that the claimed embodiments are clearly non-obvious over the four citations.

In Office Action mailed December 5, 2007, the Examiner stated that "it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper." (Page 3-4, Office Action) It is clear that the alleged motivation took the content of Applicant's disclosure as the reasoning for combining the references. For example, the Examiner uses the reason of "it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the crystal oscillator of Robinson et al. to the analog ground in order to minimize noise" (page 6, Office Action). In the present application, Applicant teaches that "by connecting a ground reference of the joint clock source that is the crystal oscillator 350 in the preferred embodiment of the present invention to the analog ground reference 360, a circuit element interference within the TDD transceiver is greatly reduced." (see

para. [0025] of the present application). Thus, it is clear that the Office Action, considered the content of Applicant's disclosure in combining the references. Such an approach is improper and consequently the rejection should be withdrawn.

In addition, Applicant continued to traverse the tenuous combination of the four references as being improper. Applicant hereby preserves this basis for traversing the rejection for appeal, should an appeal become necessary. However, based on substantive distinctions set out below, Applicant hopes that such will not be required.

In addition, in forming the rejection, the Examiner asserts that the claimed switch has been disclosed by the diplexer 36 by Isley. Applicant respectfully disagrees with this application of the cited art. In this regard, Applicant submits that the Examiner has incorrectly interpreted the diplexer 36 as the switch of the claimed embodiments.

In para [0022], lines 10-15 of the present application, it is emphasized that the switch 310 connects the antenna 305 to the down-converter 315 during a receiving data time period, and connects the antenna 305 to the up-converter 320 during a transmitting data time period. In contrast, in column 5, lines 17-21 of Isley, Jr. et al., the diplexer 36 employs a dual bandpass filter, not shown, with one filter tuned to the transmit band the other filter turned to the receive band of frequency. According to the description, It is apparent that the diplexer does not have the function of the switch of the claimed embodiments connecting the antenna to the down-converter or up-converter based on the receiving or transmitting data time period.

For at least the foregoing reasons, Isley, Jr. et al. and Robinsion et al. do not teach or suggest the switch of claims 1 and 9.

Further still, with regard to the amended claim 1, the synthesizer is coupled to a baseband processor and comprises a voltage controller oscillator. However, in the Fig. 1 of Isley, the synthesizer 24 does not contain a voltage controller oscillator and is not coupled to a baseband processor. Furthermore, in the description of columns 4 and 5, Isley does not disclose the connection between the baseband processor and the synthesizer 24, and the voltage controller oscillator. For at least this additional reason, Isley, Jr. et al. does not teach or suggest the synthesizer defined in independent claims 1 and 9.

Turning now to the specific claims, independent claims 1 and 9 (as amended herein) recite:

1. A method of minimizing a circuit element interference and stabilizing a performance of a circuit element within a Time Division Duplex (TDD) transceiver, which comprises:
  - providing a medium for a communication signal propagating back and forth through the medium;
  - constructing an analog circuit for receiving and transmitting the communication signal through the medium at a time, and for modulating and demodulating the communication signal during a communication signal receiving and transmitting process;
  - constructing a digital circuit for digital signal processing;
  - constructing an analog-to-digital (A/D) interface and a digital-to-analog (D/A) interface so that the interfaces couples the analog circuit and the digital circuit together;
  - providing a first ground reference so that all ground references of circuit elements in the analog circuit, in the A/D interface, and in the D/A interface are connected to the first ground reference;
  - providing a second ground reference so that all ground references of circuit elements in the digital circuit are grounded to the second ground reference;
  - providing a switch for transmitting or receiving the communication signal in different time periods;***
  - providing a down-converter for converting the received communication signal to a baseband signal; providing an up-

converter for converting a baseband signal to a radio frequency signal;

***constructing a synthesizer coupled to a baseband processor, comprising a voltage controller oscillator to provide the down-converter and the up-converter with a base frequency of signal so that the received and baseband communication signals are demodulated and modulated, respectively;*** and

providing a joint clock source for supplying clock pulses to the analog circuit, the digital circuit, the A/D interface, and the D/A interface, wherein the joint clock source has a ground reference directly connecting to the first ground reference and without directly connecting to the second ground reference.

9. A circuit architecture for minimizing a circuit element interference and stabilizing a performance of a circuit element within a TDD transceiver, which comprises:

a medium within which a communication signal propagates through;

an analog circuit for receiving and transmitting the communication signal in different time periods, and for modulating and demodulating the communication signal during a communication signal transmitting and receiving process;

a digital circuit for digital signal processing; an A/D interface circuit and a D/A interface circuit for coupling the analog circuit and the digital circuit together;

a first ground reference on which all ground references of circuit elements of the analog circuit, the A/D interface circuit, and the D/A interface circuit are connected together;

a second ground reference on which all ground references of circuit elements of the digital circuit are connected together;

***a switch for transmitting or receiving the communication signal in different time periods;***

a down-converter for converting the received communication signal to a baseband signal;

an up-converter for converting a baseband signal to a radio frequency signal;

***a synthesizer coupled to a baseband processor, comprising a voltage controller oscillator to provide the down-converter and the up-converter with a base frequency of signal so that the received and baseband communication signals are demodulated and modulated, respectively;*** and

a joint clock source to supply clock pulses to the analog circuit, the digital circuit, the A/D interface circuit, and the D/A interface circuit, and to have a ground reference of the joint clock source directly connected to the

first ground reference and not directly connected to the second ground reference.

*(Emphasis added)*. Independent claims 1 and 9 patently define over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

For the reasons stated above, it is Applicant's belief that all the limitations of instant claim 1 or 9 of the present application are not disclosed by the citations. It is therefore Applicant's belief that instant claims 1 and 9 are allowable over the cited reference. Insofar as all claims depend from instant claims 1 and 9, it is Applicant's belief that these claims are also in condition for allowance.

### **CONCLUSION**

This application is now in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this submission. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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